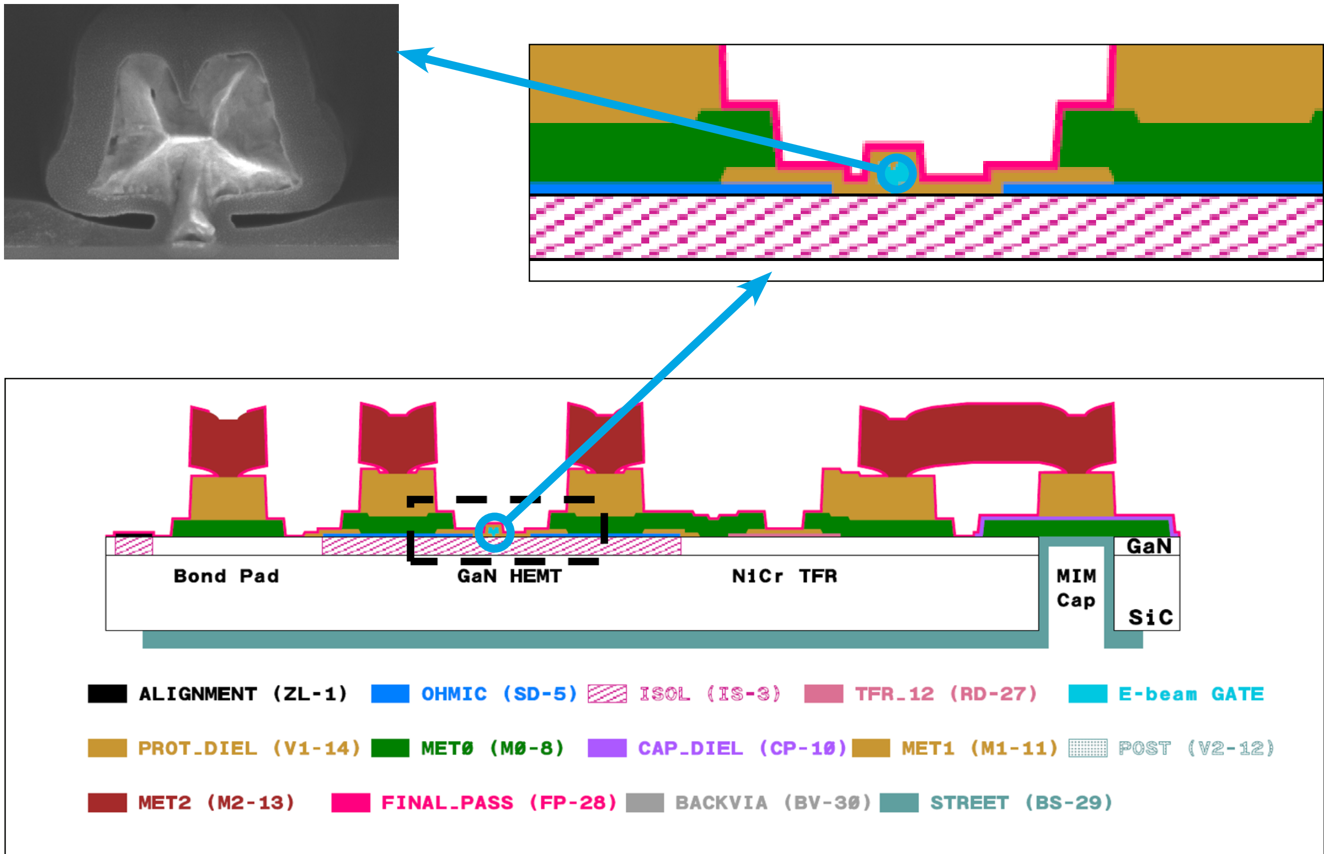
GSiC140: 0.14 µm GaN HEMT – Foundry Process



The GSiC140 process is a 0.14 µm gate length GaN-on-SiC process which utilizes E-Beam lithography for gate formation. The T-gate process features a high performance depletion mode GaN HEMT FET on a 100 µm thick SiC substrate with through VIA holes. Passives include three stackable metal layers with a total thickness of 6.46 µm, NiCr thin film and EPI (bulk) resistors, and MIM capacitors for full MMIC integration.

This highly competitive process is ideal for both commercial and defense applications from X-Band to Ka-Band.

FEATURES

- 3 Stackable Metal Layers (0.96 µm, 2.35 µm, 3.15 µm), Total Thickness: 6.46 µm
- Backside VIA: 30 x 60 µm Oval VIAs
- Final Wafer Thickness: 100 µm
- Switch FET and ESD Diodes Available
- Thin Film and Bulk Resistors
- CAP and CAP on VIA Options

APPLICATIONS

- X-Band to K-Band
- High Power Amplifiers
- High Power Switches
- Low Noise Amplifiers
- Integrated Front End MMIC

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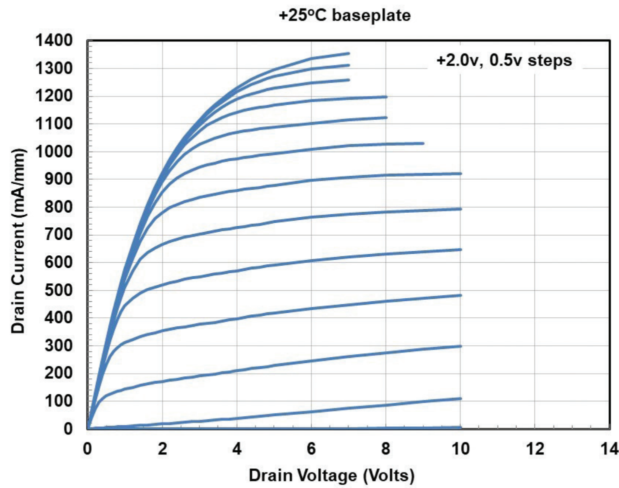
GSiC140: 0.14 µm GaN HEMT – Foundry Process (continued)

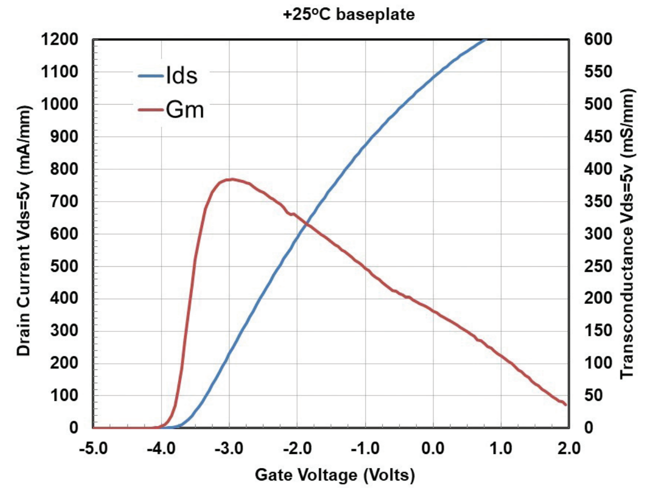
KEY PROCESS PARAMETERS

Parameter	Nominal Value
Max Drain Voltage	25 V
Pinchoff Voltage (V_{DS} = 6, I_{DS} = 1mA/mm)	-3.8 V
I_{DSS} (V_{GS} = 0 V, V_{DS} = 6 V)	960 mA/mm
I_{MAX} (I_{GS} = 1mA/mm, V_{DS} = 6 V)	1300 mA/mm
Power Density	5 W/mm @ 35 GHz
Cutoff Frequency, f_T (I_{DS} = 100 mA/mm, V_{DS} = 20 V)	>55 GHz
Transconductance, g_m (I_{DS} = 50% I_{DSS}, V_{DS}= 6 V)	375 mS/mm
Breakdown (Gate-drain, 1 mA/mm)	<-50 V
MIM Capacitance per Area	300 pF/mm²
Bulk (EPI) Resistor	300 Ω/sq
Thin Film (NiCr) Resistor	12.5 Ω/sq

GSiC140: 0.14 µm GaN HEMT – Foundry Process (continued)

Typical Performance Curves
DC Characteristics

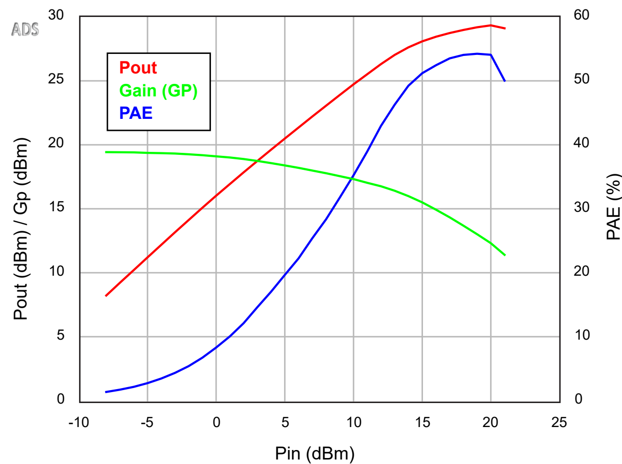




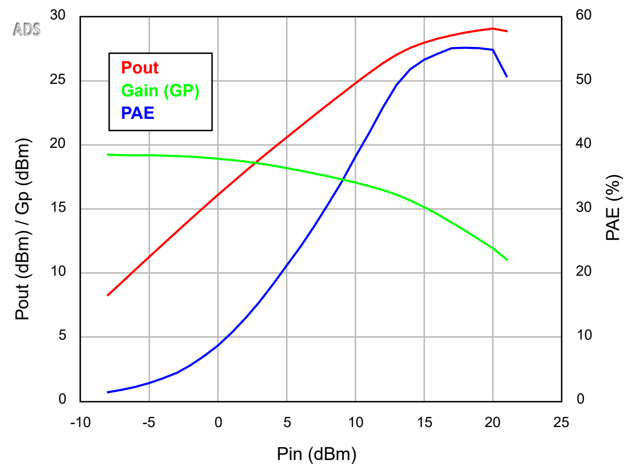
Typical Performance Curves
Load Pull (2 x 100 µm FET)

10 GHz (V_{DS} = 25 V, I_{DSQ} = 100 mA/mm)

Peak Power Tune



Peak Efficiency Tune



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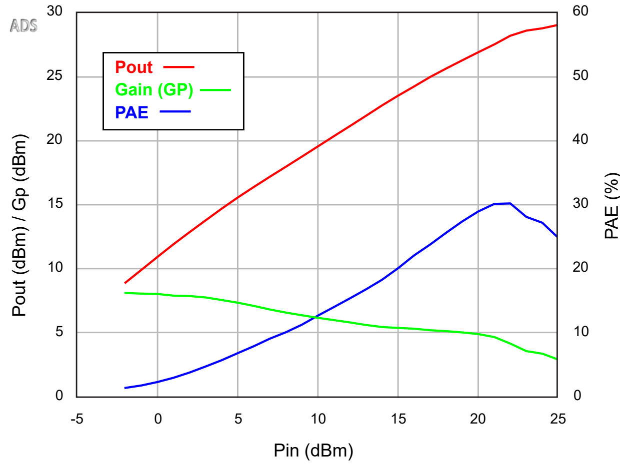
GSiC140: 0.14 µm GaN HEMT – Foundry Process (continued)

Typical Performance Curves
Load Pull (2 x 100 µm FET)

30 GHz (V_{DS} = 25 V, I_{DSQ} = 100 mA/mm)

Peak Power Tune



Peak Efficiency Tune